(f) isotropically etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate dielectric layer; and

(g) forming a first impurity layer and a second impurity layer by ion-implanting an impurity in the semiconductor substrate,

wherein an extension region is formed in the semiconductor substrate below the extension control layer during the ion-implanting used to form the first impurity layer and the second impurity layer.

2. (amended) A method for manufacturing a semiconductor device according to claim 1, wherein the step (f) further includes the step of forming a sidewall protection layer on sidewalls of the gate electrode.

3. (amended) A method for manufacturing a semiconductor device according to claim 2, further including removing the sidewall mask layer after the isotropically etching the dielectric layer and prior to the forming a first impurity layer and a second impurity layer.

21. (amended) A method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a gate electrode over the gate dielectric layer;

forming extension control structures over a portion of the semiconductor substrate next to the gate dielectric layer by forming a dielectric layer on the semiconductor substrate, forming a mask layer on the dielectric layer, anisotropically etching the mask layer to form a sidewall mask layer, and isotropically etching the dielectric layer after forming the sidewall mask layer; and

an ion-implanting step that forms extension regions in the semiconductor substrate under the extension control structures and source/drain regions in the semiconductor substrate adjacent to the extension layer, wherein the extension regions have a depth that is less than that of the source/drain regions.

22. (amended) A method according to claim 21, further comprising forming sidewall protection structures on sidewalls of the gate electrode during the isotropically etching the dielectric layer.

23. (amended) A method according to claim 22, further comprising removing the sidewall mask layer prior to the ion-implanting.

24. (amended) A method of manufacturing a semiconductor device according to claim 1, wherein the extension control layer is formed from silicon nitride and the sidewall mask is formed from silicon oxide.

Please add new claims 25-26 as follows:

--25. (new) A method according to claim 21, wherein the ion-implanting step is carried out as a single ion-implantation operation.

26. (new) A method according to claim 22, wherein the extension control layer and the sidewall protection layer are formed from silicon nitride and the sidewall mask layer is formed from silicon oxide.--

REMARKS

Applicant has amended claims 1-3 and 21-24, canceled claims 10-20 without prejudice, and added new claims 25-26. Claims 1-9 and 21-26 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 10-20 have been canceled with prejudice to prosecute these claims at a later time.

In the drawings, applicant proposes to insert the terms "Prior Art" to Figs. 5-6 as suggested by the Examiner and as illustrated in red on the attached sheets. Applicant will submit formal drawings after the amendment has been approved.